

Subst. Form PTO-1449  APPLICANT'S INFORMATION DISCLOSURE STATEMENT	Atty. Docket No.: RPS920030157US1 (IRA-20-5829)	Serial No.: To be assigned
	Applicant: Basso et al	
	Filing Date: Herewith	Group: To be assigned

## U.S. PATENT DOCUMENTS

Initial*		Document No.	Date	Name	Class	Subcl.	Filing Date
/A.R./	AA	5,835,745	11/10/1998	Sager et al	395	391	03/07/1996
/A.R./	AB	5,845,072	12/01/1998	Finney et al	395	200.38	05/05/1997
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/A.R./	AH						

## FOREIGN PATENTS

		Document No.	Date	Country	Class	Subcl.	Translation?
/A.R./	AI	JP11203145A	07/30/1999	Japan			Abstract attached
/A.R./	AJ	JP20022334126A	11/22/2002	Japan			Abstract attached

## OTHER DOCUMENTS

/A.R./	AK	IBM Technical Disclosure Bulletin, Vol. 36, No. 12, "Compute-Send-Receive -> Sequence Processing within the Multisequencing in a Single Instruction Stream Scheduler", December, 1993, pp 3-8
/A.R./	AL	INSPEC - (Chatha et al; 1998) - two articles; (Wakabayashi et al; 1992); Chatha et al; 2001) Dave et al; 1998/1997) - two articles, 7 pages
/A.R./	AM	"Efficient Longest Executable Path Search for Programs with Complex Flows and Pipeline Effects", Stappert et al, 2001, pp 132-140
/A.R./	AN	"SCED: A Generalized Scheduling Policy for Guaranteeing Quality-of-Service", Sariowan et al, IEEE/ACM Transactions on Networking, Vol. 7, No. 5, October, 1999, pp 669-684
/A.R./	AO	"RECOD: A Retiming Heuristic To Optimize Resource And Memory Utilization in HW/SW Codesigns", Chatha et al, Proceedings of the Sixth International Workshop on Hardware / Software Codesign, IEEE Computer Society et al, March 15-18, 1998, pp 139-143
/A.R./	AP	"MAGELLAN: Multiway Hardware-Software Partitioning and Scheduling for Latency Minimization of Hierarchical Control-Dataflow Task Graphs", Chatha et al, Proceedings of the Ninth International Symposium on Hardware/Software Codesign, ACM SIGDA et al, April 25-27, 2001, pp 42-47
/A.R./	AQ	"COHRA: Hardware-Software Co-Synthesis of Hierarchical Distributed Embedded System Architectures", Dave et al, Proceedings of the Eleventh International Conference on VLSI Design, VLSI Society of India, January 4-7, 1998, pp 347-354

Examiner: /Abdulla Riyami/	Date Considered: 11/15/2007
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if in conformance and not considered.  
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RPS920030157US1 (IRA-10-5829)

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/A.R./	AK	"A Synthesis Algorithm for Pipelined Data Paths with Conditional Module Sharing", Wakabayashi et al, 1992 IEEE International Symposium on Circuits and Systems, Volume 2 of 6, IEEE, May 10-13, 1992, pp 677-680
/A.R./	AL	"COHRA: Hardware-Software Cosynthesis of Hierarchical Heterogeneous Distributed Embedded Systems", Dave et al, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 17, No. 10, October, 1998, pp 900-919
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